

Vertical cross phase demodulation circuit

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Abstract of TW 462168 (B)

In the vertical cross phase demodulation circuit, a simple circuit is used to eliminate DC offset. When a clock reproduction circuit 6 is locked, a phase comparator 9 detects a level difference $[\Delta]E$ between a zero crossing point and a true 0 level. The level difference $[\Delta]E$ represents an offset level and maintains the level difference $[\Delta]E$ of the original level output. After being flattened by the LPF 12, the level difference $[\Delta]E$ is input to adders 14 and 15 so as to eliminate a DC offset.

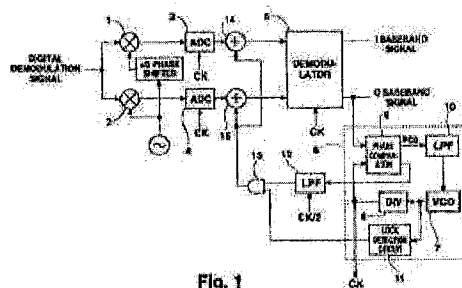


Fig. 1

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